

Description

The XPX400N10LL uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.

General Features

- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high E_{AS}
- Excellent package for good heat dissipation

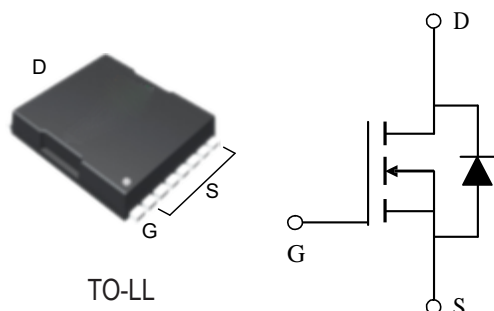
Application

- PWM
- Load Switching

$$V_{DS} = 100V, I_D = 400A$$

$$R_{DS(ON)} = 1.0m\Omega \text{ (typ) @ } V_{GS} = 10V$$

$$R_{DS(ON)} = 1.8m\Omega \text{ (typ) @ } V_{GS} = 6.0V$$



Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	Drain-Source Voltage	$T_C = 25^\circ C$	100	-	V
V_{GS}	Gate-Source Voltage	$T_C = 25^\circ C$	-	± 20	V
I_D^*	Drain Current (DC)	$T_C = 25^\circ C, V_{GS} = 10V$	-	400	A
		$T_C = 100^\circ C, V_{GS} = 10V$	-	290	A
$I_{DM}^{*, **}$	Drain Current (Pulsed)	$T_C = 25^\circ C, V_{GS} = 10V$	-	1668	A
P_D	Power Dissipation	$T_C = 25^\circ C$	-	430	W
I_S	Continuous-Source Current	$T_C = 25^\circ C$	-	417	A
E_{AS}	Single Pulsed Avalanche Energy	$V_{DD} = 50V, L = 0.5mH$	-	1750	mJ
T_J, T_{stg}	Operating Junction and Storage Temperature Range		-55	175	$^\circ C$
$R_{\theta JA}^{**}$	Thermal Resistance-Junction to Ambient		-	40	$^\circ C/W$
$R_{\theta JC}^{**}$	Thermal Resistance-Junction to Case		-	0.35	$^\circ C/W$

Device	Pack	Marking	Qty(PCS)
XPX400N10LL	TOLL	XPX400N10LLXXXX YYYY	2000

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0 V, I _{DS} =250 μA	100	-	-	V
V _{GS(TH)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _{DS} =250 μA	2.2	-	3.5	V
I _{DSS}	Drain Leakage Current	V _{DS} =100 V, V _{GS} =0 V	-	-	1	μA
I _{GSS}	Gate Leakage Current	V _{DS} =0 V, V _{GS} =±20 V	-	-	±100	nA
R _{DS(ON)} ^a	On-State Resistance	V _{GS} =10 V, I _{DS} =50 A	-	1.1	1.3	mΩ
		V _{GS} =6 V, I _{DS} =30 A	-	1.3	1.8	mΩ
g _{fs}	Forward Transconductance	V _{DS} =5 V, I _{DS} =30 A	-	49	-	S
R _g	Gate Resistance		-	1	2	Ω
Diode Characteristics						
V _{SD} ^a	Diode Forward Voltage	V _{GS} =0 V, I _{SD} =30 A	-	0.8	1.1	V
t _{rr}	Reverse Recovery Time	V _{DS} =50 V, V _{GS} =0 V, I _{DS} =30 A, di/dt=100 A/μs	-	113	-	ns
Q _{rr}	Reverse Recovery Charge		-	400	-	nC
Dynamic Characteristics ^b						
C _{iss}	Input Capacitance	V _{DS} =50 V, V _{GS} =0 V, f=1 MHz	-	16500	-	pF
C _{oss}	Output Capacitance		-	2110	-	
C _{rss}	Reverse Transfer Capacitance		-	380	-	
t _{d(on)}	Turn-on Delay Time	V _{DS} =50 V, V _{GEN} =10 V, R _G =6 Ω, I _{DS} =30 A	-	65	-	ns
t _r	Turn-on Rise Time		-	60	-	
t _{d(off)}	Turn-off Delay Time		-	223	-	
t _f	Turn-off Fall Time		-	104	-	
Gate Charge Characteristics ^b						
Q _g	Total Gate Charge	V _{DS} =50 V, V _{GS} =10 V, I _{DS} =30 A	-	260	-	nC
Q _{gs}	Gate-Source Charge		-	65	-	
Q _{gd}	Gate-Drain Charge		-	70	-	

Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

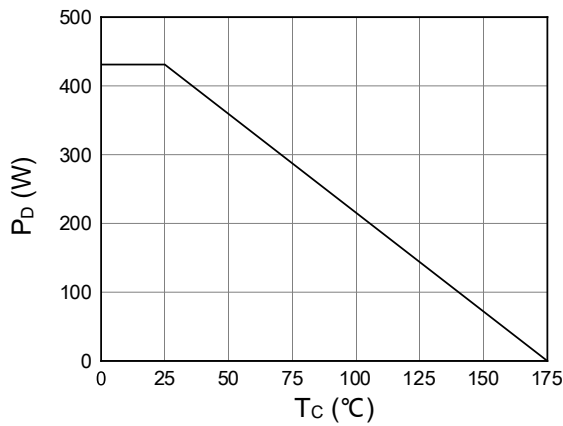


Figure 1. Power Capability

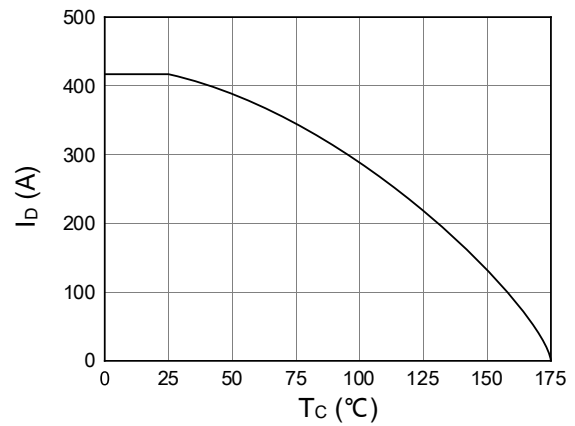


Figure 2. Current Capability

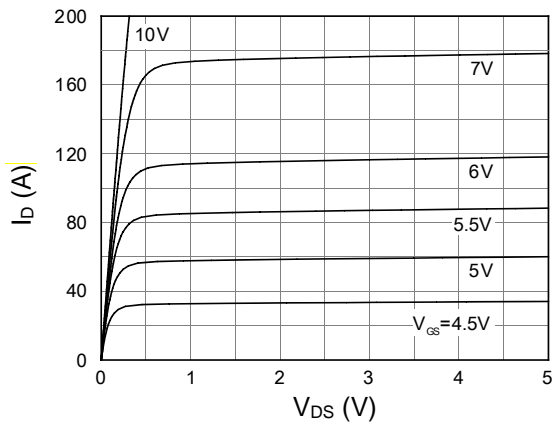


Figure 3. Output characteristics

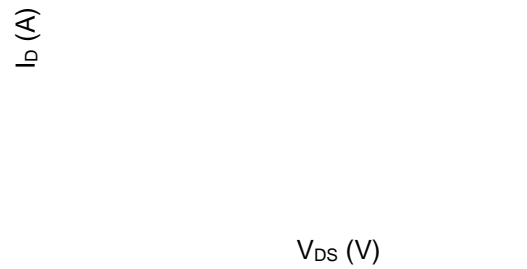


Figure 4. Safe operating area

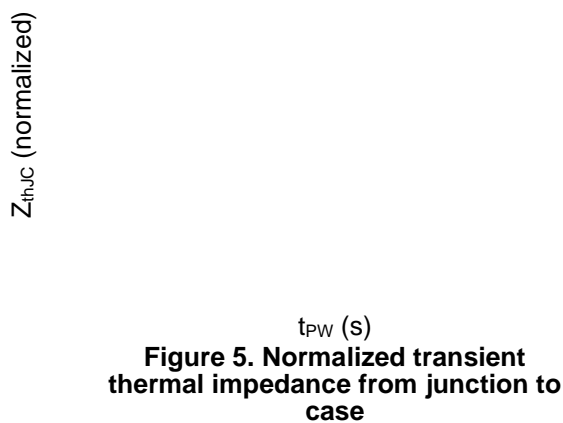


Figure 5. Normalized transient thermal impedance from junction to case



Figure 6. Normalized on-resistance vs drain current

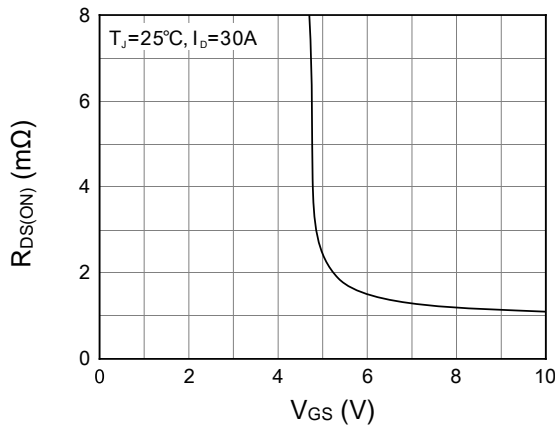


Figure 7. On-resistance vs gate-source voltage

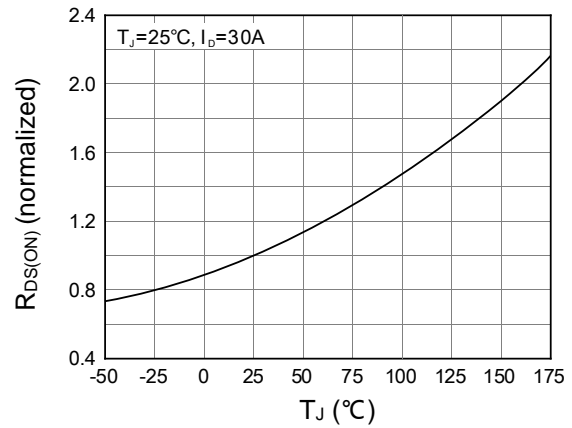


Figure 8. Normalized on-resistance vs junction temperature

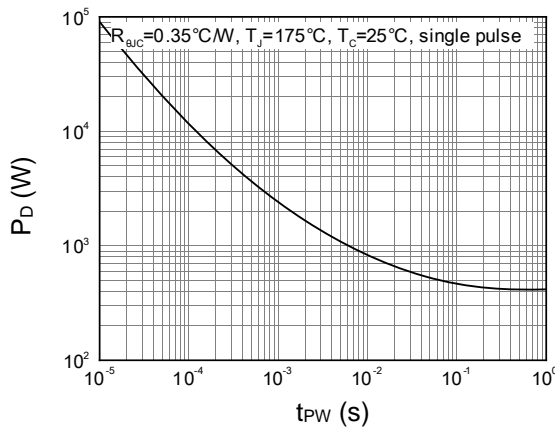


Figure 9. Single pulse maximum power dissipation

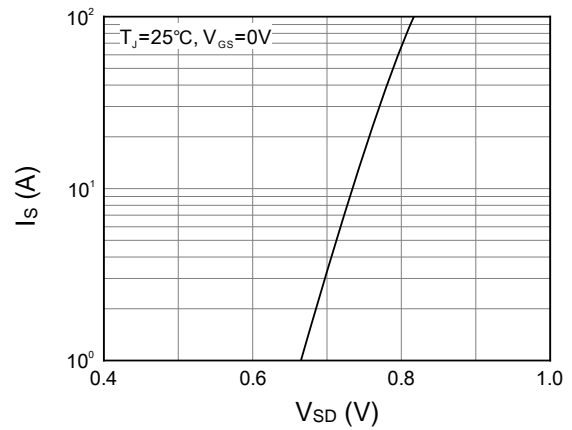


Figure 10. Forward characteristics of body diode

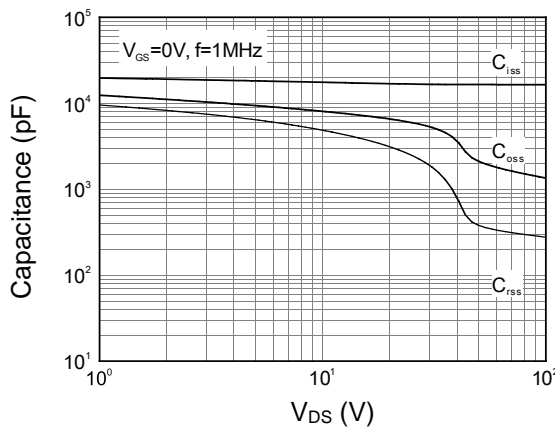


Figure 11. Capacitance

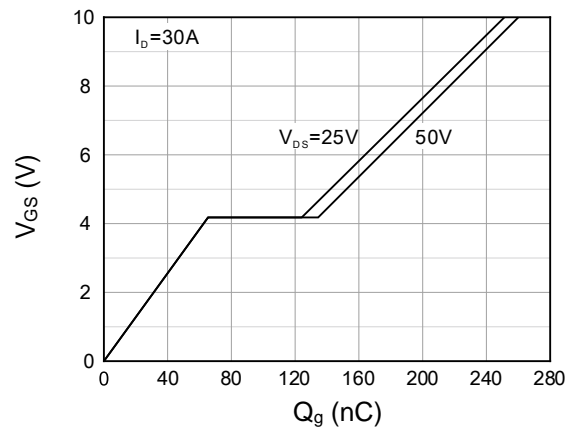
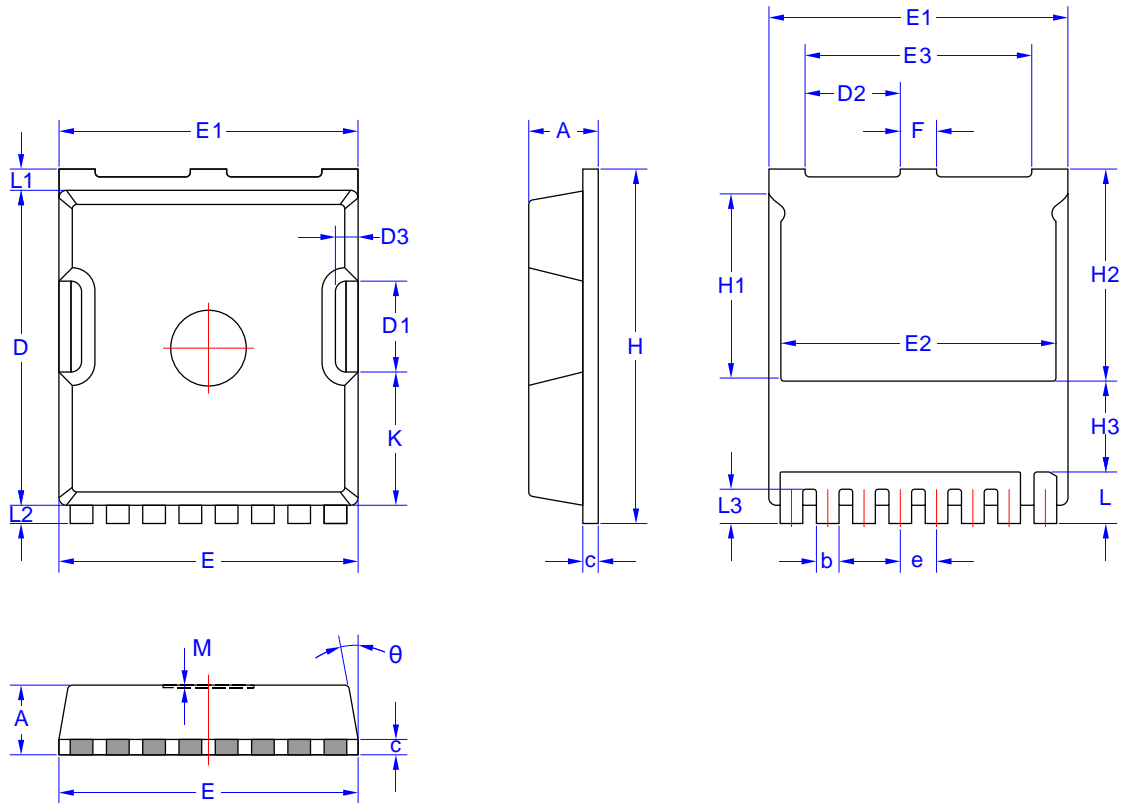


Figure 12. Gate charge

TOLL-8L Package


Symbol	Dimensions in Millimeters		
	MIN	NOM	MAX
A	2.20	2.30	2.40
b	0.65	0.75	0.85
c		0.508 REF	
D	10.25	10.40	10.55
D1	2.85	3.00	3.15
D2	2.95	3.10	3.25
D3		0.75 REF	
E	9.75	9.90	10.05
E1	9.65	9.80	9.95
E2	8.95	9.10	9.25
E3	7.25	7.40	7.55
e		1.20 BSC	

Symbol	Dimensions in Millimeters		
	MIN	NOM	MAX
F	1.05	1.20	1.35
H	11.55	11.70	11.85
H1	6.03	6.18	6.33
H2	6.85	7.00	7.15
H3		3.00 BSC	
K	4.25	4.40	4.55
L	1.55	1.70	1.85
L1	0.55	0.70	0.85
L2	0.45	0.60	0.75
L3	1.00	1.15	1.30
M		0.08 REF	
θ	8°	10°	12°

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245°C \pm 5°C	5sec \pm 1 sec
Pb-Free device	260°C \pm 0/-5°C	5sec \pm 1 sec



This integrated circuit can be damaged by ESD. UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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